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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,053	05/20/2000	Frank W. Ahern	101950-00027	9991

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Robert C. Klinger
Jackson Walker, LLP
Suite 600
2435 N. Central Expressway
Richardson, TX 75080

MAIL DATE CANCELLER

EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,053	AHERN, FRANK W.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-52 and 54-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *54-59* is/are allowed.

6)☒ Claim(s) *24-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 24-52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 24 and 31 are rejected because it is not clear if the same data is being transferred in two different data transactions. Applicant refers to transferring "bus data as a data transaction" and then also recites transferring "the bus data as another data transaction". Is the same bus data being referred to in both places?

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 24-42,44-47,50 and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Vicard et al., U.S. Pat. No. 6,003,105 (previously cited).

As per claim 24, Vicard shows an interface comprising a circuit adapter to couple a first bus having a parallel data bus (fig.4,40), the circuit adapted to serially send the bus data as a data transaction over a link (124) to a physically remote second bus (140) without requiring or waiting for an incoming acknowledgement over the link before inaugurating a transfer of the bus

data as another data transaction over the link (col.3, line 60-col.4, line 45 and col.5, lines 10-15 which explains that the PCI transactions are handled transparently with no need to adapt any hardware or software). Vicard shows all of the limitations recited in claim 24.

As for claim 25, the argument for claim 24 applies. Vicard also shows that the first bus is a PCI bus (col.4, line 65). Vicard shows all of the limitations recited in claim 25.

As for claim 26, the argument for claim 24 applies. Vicard also shows that the circuit is an integrated circuit (inherent in modern electronic and computer components). Vicard shows all of the limitations recited in claim 26.

As for claim 27, the argument for claim 26 applies. Vicard also shows that the integrated circuit is an application specific integrated circuit (ASIC)(also inherent in modern electronic and computer components). Vicard shows all of the limitations recited in claim 27.

As for claim 28, the argument for claim 24 applies. Vicard also shows that the circuit is operable to exchange bus data according to a predetermined hierarchy giving the first bus a higher level than the second bus (inherent in the PCI bridge, see at least PCI to PCI Bridge Architecture Specification section 5). Vicard shows all of the limitations recited in claim 28.

As for claim 29, the argument for claim 24 applies. Vicard also shows a first register adapted to hold parallel bus data (the buffers in figure 2 and discussed in cols. 3-4). Vicard shows all of the limitations recited in claim 29.

As for claim 30, the argument for claim 29 applies. Vicard also shows a second register adapted to hold received second bus data (the buffers in figure 2 and discussed in cols. 3-4). Vicard shows all of the limitations recited in claim 30.

As per claim 31, Vicard shows a bridge accessible by a processor for expanding access over a first bus (40) to a second bus (140), said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices (figs.

3-5), said bridge comprising: a link (124); a first interface coupled between said first bus and said link (21); and a second interface adapted to couple between said second bus and said link (121), said first interface and said second interface being operable to transfer bus data as a data transaction serially through said link without waiting for an incoming acknowledgment over said link before inaugurating a transfer of the bus data as another data transaction over said link (col.3, line 60-col.4, line 45 and col.5, lines 10-15 which explains that the PCI transactions are handled transparently with no need to adapt any hardware or software). Vicard shows all of the limitations recited in claim 31.

As for claim 32, the argument for claim 31 applies. Vicard also shows that the first and second interfaces are operable to exchange bus data according to a predetermined hierarchy giving the first bus a higher level than the second bus (inherent in the PCI bridge, see at least PCI to PCI Bridge Architecture Specification section 5). Vicard shows all of the limitations recited in claim 32.

As for claim 33, the argument for claim 31 applies. Vicard also shows that said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface being operable in response to a pending transaction on said first bus to begin processing said pending transaction and to apply a retry signal to at least one of said signaling lines of said first bus before the pending transaction on said first bus has been transmitted to and acknowledged by said second bus (inherent in PCI bus operation). Vicard shows all of the limitations recited in claim 33.

As for claim 34, the argument for claim 33 applies. Vicard also shows that less than all of the information on the signaling lines of said first bus is transmitted by said first interface over said link (inherent in PCI bridge operation). Vicard shows all of the limitations recited in claim 34.

As for claim 35, the argument for claim 31 applies. Vicard also shows that said first interface is selectively responsive to those addresses appearing on said first bus that are on a predetermined schedule of addresses corresponding to the bus-compatible devices accessible through said second bus, in order to avoid responding to addresses corresponding to other ones of the bus-compatible devices on said first bus (inherent in the PCI bridge, which includes address registers and configuration as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Vicard shows all of the limitations recited in claim 35.

As for claim 36, the argument for claim 35 applies. Vicard also shows a register for storing the predetermined schedule (inherent in the PCI bridge, which includes base address registers as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Vicard shows all of the limitations recited in claim 36.

As for claim 37, the argument for claim 35 applies. Vicard also shows that said first interface comprises: a first register for storing said predetermined schedule, said second interface comprising: a second register for storing said predetermined schedule (inherent in the PCI bridge, which includes base address registers as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Vicard shows all of the limitations recited in claim 37.

As for claim 38, the argument for claim 36 applies. Vicard also shows that said register is operable to establish with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus (inherent in the PCI bridge, which includes base address registers as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Vicard shows all of the limitations recited in claim 38.

As for claim 39, the argument for claim 31 applies. Vicard also shows a register for establishing with respect to the first bus a base address for one or more of the bus compatible devices on the second bus (inherent in the PCI bridge, which includes base address registers

as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Vicard shows all of the limitations recited in claim 39.

As for claim 40, the argument for claim 31 applies. Vicard also shows that the first interface and second interface are operable to permit communication between bus compatible devices on the second bus without routing through the first bus (inherent in the PCI bridge, wherein transactions that are only within the address range of devices on the second bus are not passed through the bridge, see PCI to PCI Bridge Architecture Specification section 6.1). Vicard shows all of the limitations recited in claim 40.

As for claim 41, the argument for claim 31 applies. Vicard also shows that said first interface and said second interface comprise: a first and a second programmable logic device connected between said link and said first bus and said second bus, respectively (figs. 2 and 4). Vicard shows all of the limitations recited in claim 41.

As for claim 42, the argument for claim 31 applies. Vicard also shows that said first interface and said second interface comprise: a first and a second application-specific integrated circuit connected between said link and said first bus and said second bus, respectively (figs. 2 and 4). Vicard shows all of the limitations recited in claim 42.

As for claim 44, the argument for claim 42 applies. Vicard also shows that the first and second application-specific integrated circuits each comprise a plurality of ports configured to provide input/output of the bus data (figs. 2 and 4). Vicard shows all of the limitations recited in claim 44.

As for claim 45, the argument for claim 31 applies. Vicard also shows that said processor is interrupt-driven, said second interface being operable to transmit through said link to said first interface interrupt signals destined to interrupt the processor (inherent in PCI

operation, see PCI to PCI Bridge Architecture Specification section 11). Vicard shows all of the limitations recited in claim 45.

As for claim 46, the argument for claim 45 applies. Vicard also shows that said processor is responsive to error signals, said second interface being operable to transmit through said link to said first interface error signals destined to affect the processor (inherent in PCI operation, see PCI to PCI Bridge Architecture Specification section 8). Vicard shows all of the limitations recited in claim 46.

As for claim 47, the argument for claim 31 applies. Vicard also shows that said first bus operates at a predetermined clock speed, said link being operable to propagate data between said first interface and said second interface at a bit transfer rate greater than said predetermined clock speed (col.3, lines 36-40). Vicard shows all of the limitations recited in claim 47.

As for claim 50, the argument for claim 31 applies. Vicard also shows that the second bus is a PCI bus (at least in col.5, lines 50-52). Vicard shows all of the limitations recited in claim 50.

As for claim 52, the argument for claim 31 applies. Vicard also shows that said first interface and said second interface are operable to permit at least one of the bus-compatible devices on said second bus to address one or more of the bus-compatible devices on said first bus using on said second bus substantially the same type of addressing as is used to access devices on said second bus (abstract and cols.3-5, wherein both of the buses are PCI buses and the system is arranged such that devices one either bus can access the other bus). Vicard shows all of the limitations recited in claim 52.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vicard in view of Hong (previously applied).

As for claim 48, the argument above for claim 47 applies. Vicard shows a gigbit serial link (at least in fig.3) but does not specifically show that the link comprises a pair of simplex links for sending information in opposite directions. Hong shows a PCI to PCI link system with a serial link comprising a pair of unidirectional links that operate at one gigabit per second to send information in opposite directions (col. 3, lines 28-32 and fig.2, (108 or 110)). It would have been obvious to one of ordinary skill in the art at the time of the invention to use a serial link with a pair of simplex links for sending information in opposite directions as shown by Hong in the system of Vicard in order to facilitate the fast transmission of data between the interfaces.

As for claim 49, the argument for claim 48 applies. Hong also shows that the simplex links are driven for differential signal transfers (col.3,lines 28-32).

7. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vicard in view of what was well known in the art.

As for claim 51, the argument for claim 31 applies. Vicard also shows that said second interface is operable in response to a transaction from said link signifying an initial read request to fetch data from a competent one of the bus-compatible devices on said second bus for transmission back over said link in order to satisfy pending and anticipated transactions (cols. 3-

5 which includes various queues for storing data to be transmitted via the serial link to the other interface circuit). Vicard does not specifically show pre-fetching data in response to a transaction. However, Official Notice is taken that it is well known in the art to pre-fetch data in order to respond more quickly to data requests.

Response to Arguments

8. Applicant's arguments, see pages 11-12, filed 11 September 2006, with respect to the rejection(s) of claim(s) 24 and 31 under 35 USC 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Vicard as applied above in response to applicant's amendment of the claims.

Allowable Subject Matter

9. Claim 43 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 54-59 are allowed.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
13 November 2006

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